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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/767,323	01/22/2001	Lester Sanders	X-778 US	9356

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EXAMINER	
BRODA, SAMUEL	
ART UNIT	**PAPER NUMBER**
2123	2

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/767,323	SANDERS, LESTER
	Examiner	Art Unit
	Samuel Broda	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-24* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Drawings

2. Applicant's formal drawings have been reviewed and approved.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3.1 Claims 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 17 refers to "[t]he method of claim 15" but claim 15 is a product claim.

For the purpose of further examination, claim 17 will be considered to be dependent on the method of claim 16. Correction is required.

3.2 Claims 18-20 are dependent on claim 17 and are therefore also rejected.

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> ...
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Eisenmann et al, "Power Calculation for High Density CMOS Gate Array's," IEEE Euro ASIC '91, pp. 198-203 (May 1991).

4.2 Regarding claims 1 and 7-9, Eisenmann et al teaches a method for simulating operation of at least a portion of an integrated circuit for determining dynamic power dissipation associated therewith, comprising:

dividing the integrated circuit into at least one cell [H4C family of CMOS circuits divided into cell macros, page 200 column 1 paragraph 1];

identifying at least one node associated with the at least one cell [nodes correspond to primitive macros, page 200 column 1 paragraph 1, and Figs. 2-4];

providing parameters, other than frequency, for determining dynamic power dissipation of the at least one node [parameters such as external capacitances extracted from the circuit layout, page 200 column 1 paragraph 1];

simulating operation of the at least one cell [Verilog and "POWCAL" simulations, page 201 Fig.5];

counting transitions of the at least one node to provide an activity factor [activity factor corresponding to number of events "N", page 201 "Section 2.2 Toggle Frequency f"];

dividing the activity factor by simulation time to obtain the frequency [equation (5) page 201 "Section 2.2 Toggle Frequency f"]; and

calculating dynamic power dissipation for the at least one node [activity factor "N" used to determine toggle frequency "f" for use in equations (3) and (4), page 199 and page 201 "Section 2.2 Toggle Frequency f"].

Therefore, Eisenmann et al anticipates claim 1.

4.3 Regarding claims 2-6, the nodes inside the CMOS include clock nodes, data nodes, combinatorial logic nodes, sequential circuitry nodes, and toggled flip-flop nodes. See the examples in Figs. 2-4, and page 202 describing the simulation examples for a processor-controller, a video controller, and the H4C array.

4.4 Regarding claims 10-13, these claims are anticipated using the analysis of claim 1, with the transitions counted to determine the toggle frequency f in Section 2.2 of Eisenmann et al.

4.5 Regarding claims 14-15, these claims are anticipated using the analysis of claim 1, with reference to the power calculation system of Fig. 5, wherein the "POWCAL" module

produces a "macro power file" corresponding to the testbench of claim 14 and also produces a "report file" corresponding to the power dissipation code of claim 15.

4.6 Regarding claims 16-18, these claims are anticipated using the analysis of claim 1, with reference to the power calculation system of Fig. 5, wherein the "POWCAL" module determines the dynamic power dissipation. As described in "3. Prototype Implementation," the circuit data model sent to "POWCAL" is back-annotated.

4.7 Regarding claim 19, this claim is anticipated using the analysis of claim 1, with reference to the power calculation system of Fig. 5, wherein the "POWCAL" module includes multiplying static current (corresponding to "standby current") by the source voltage. See page 199 "2. Research Work" and equation (2).

Allowable Subject Matter

5.1 Claim 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

5.2 Claims 21-24 are allowed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Reference to Hamada et al, U.S. Patent 6,493,863 is cited as teaching generation of an RTL circuit described in an HDL after power consumption is minimized.

Reference to Dean et al, U.S. Patent 6,397,170 is cited as teaching a method for designing a low power ASIC using weighted net toggle information.

Reference to Sarin, U.S. Patent 5,838,947 is cited as teaching a VLSI MOS circuit design system using a power gate simulation engine connected to a power gate characterizer.

Reference to Khouja et al, U.S. Patent 5,696,694 is cited as teaching power dissipation calculations at the gate level using toggle frequency.

Reference to Rodnunsky et al, "Power Estimation of CMOS Circuits via Power Software," IEEE Canadian Conference on Electrical and Computer Engineering, Vol. 1, pp. 149-152 (May 1998), is cited as teaching dynamic power calculations using a count of switching transitions and sample period time.

Reference to Macii et al, "Power Consumption of Static and Dynamic CMOS Circuits: A Comparative Study," IEEE 2nd International Conference on ASIC, pp. 425-427 (October 1996), is cited as teaching a review of the factors to be taken into account when the choice of CMOS technology is driven by power consumption.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER